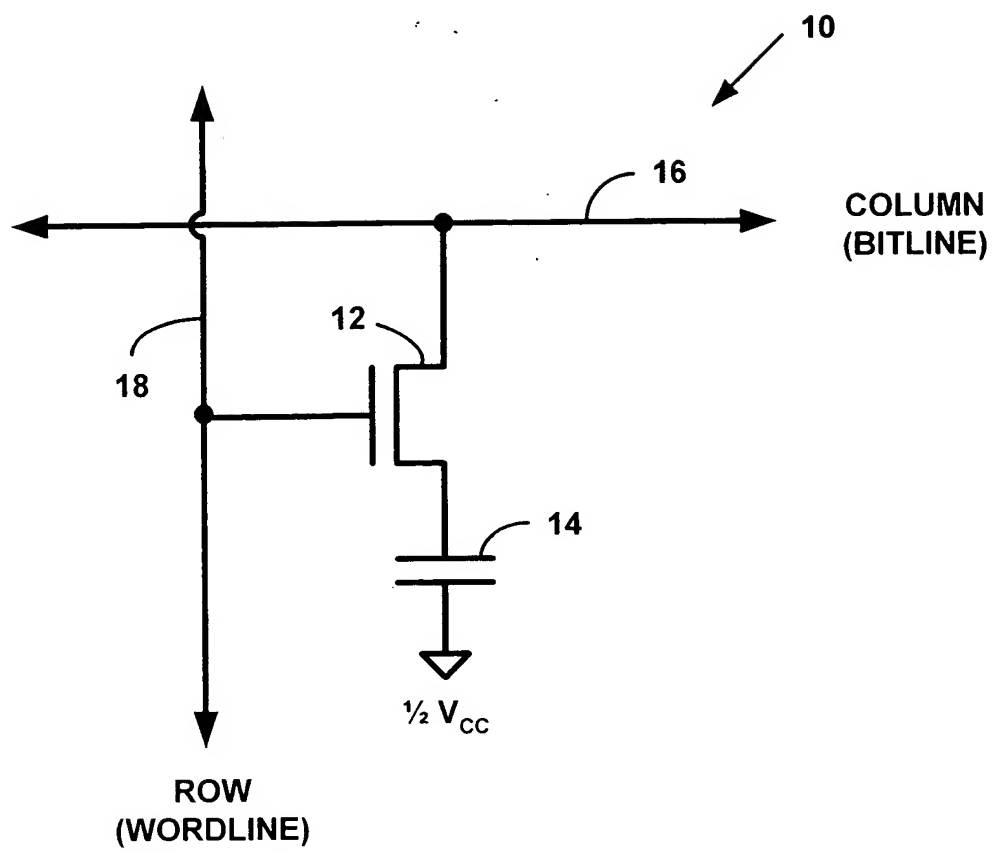


# FIG 1



# FIG 2

22

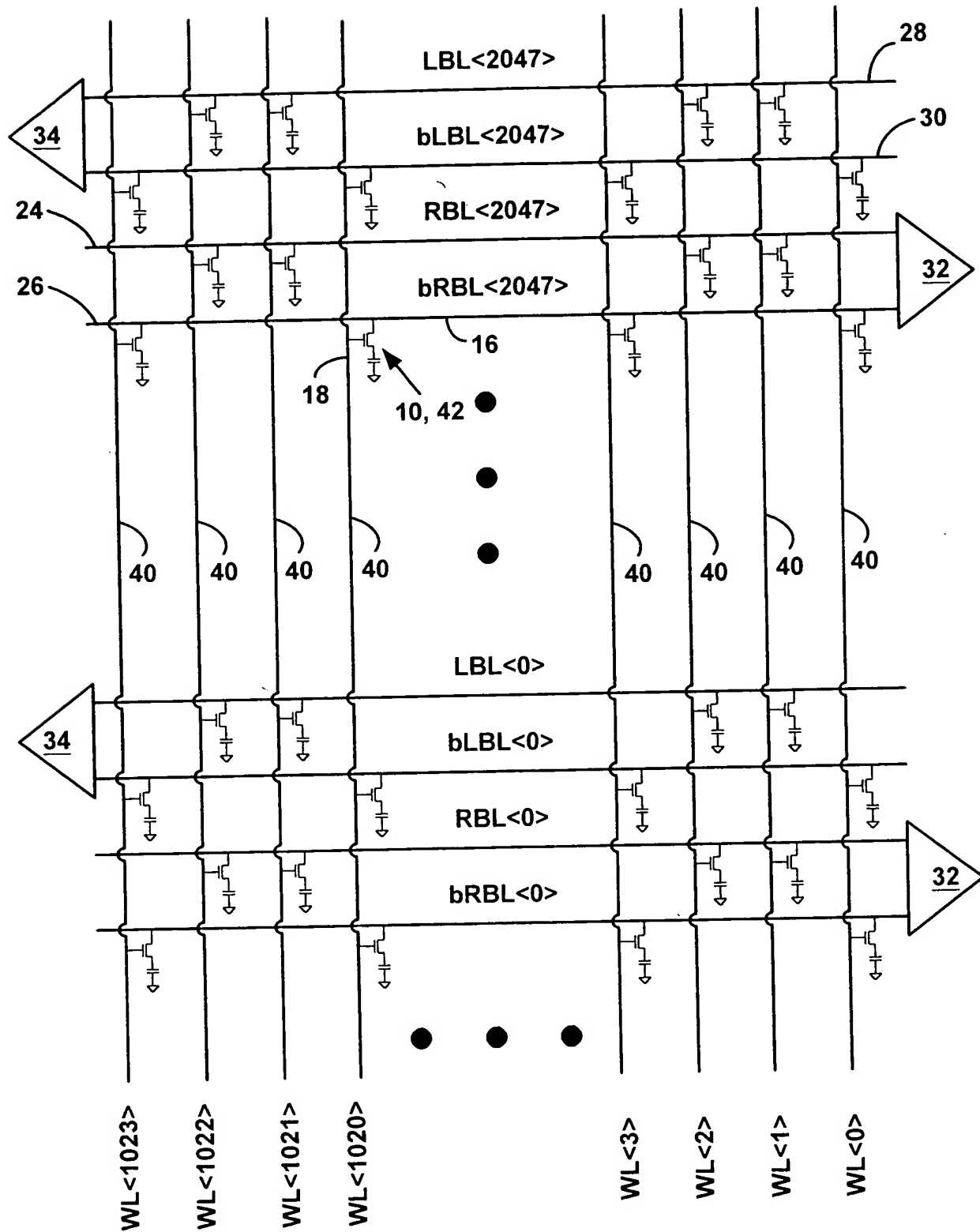


FIG. 3

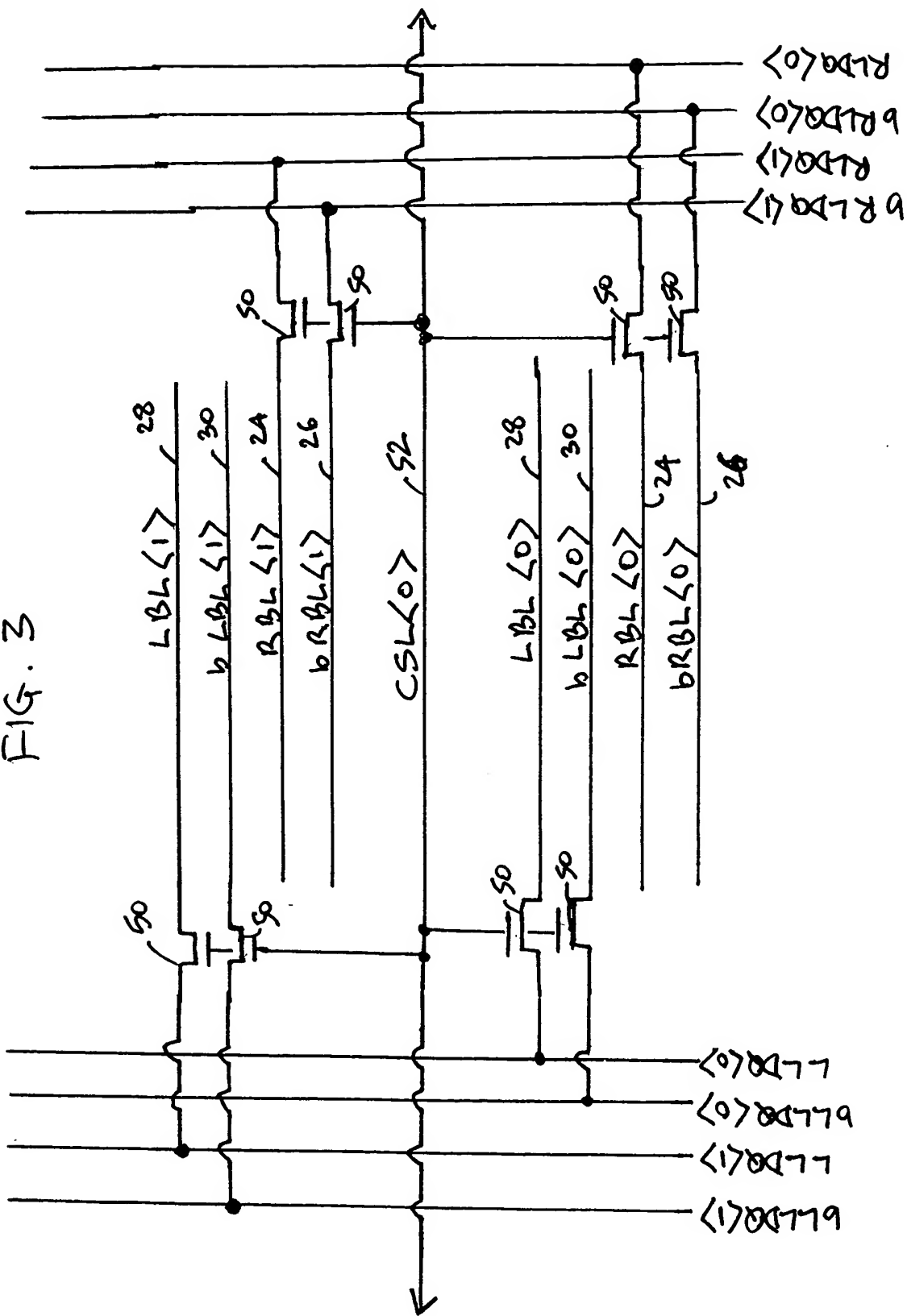
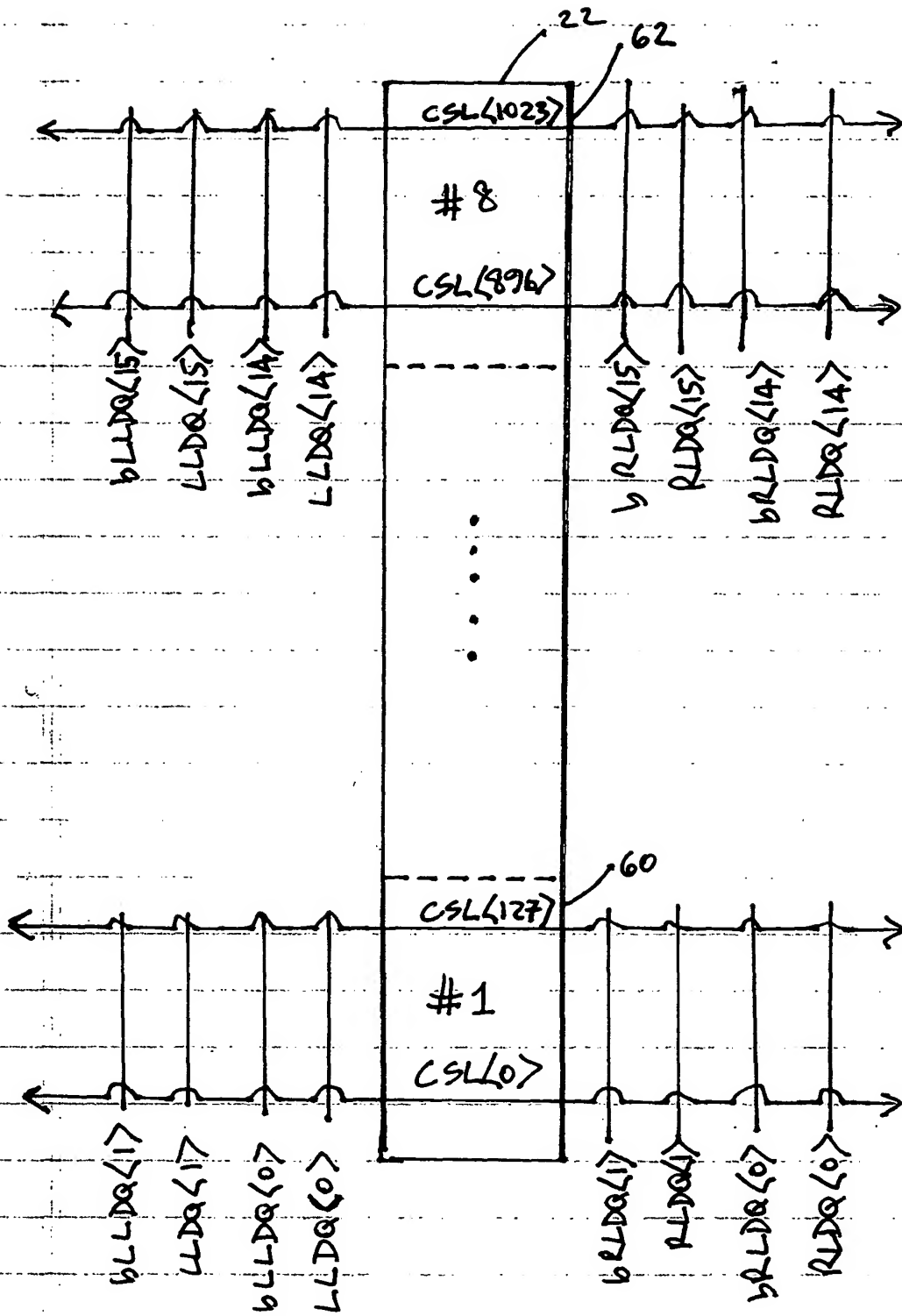
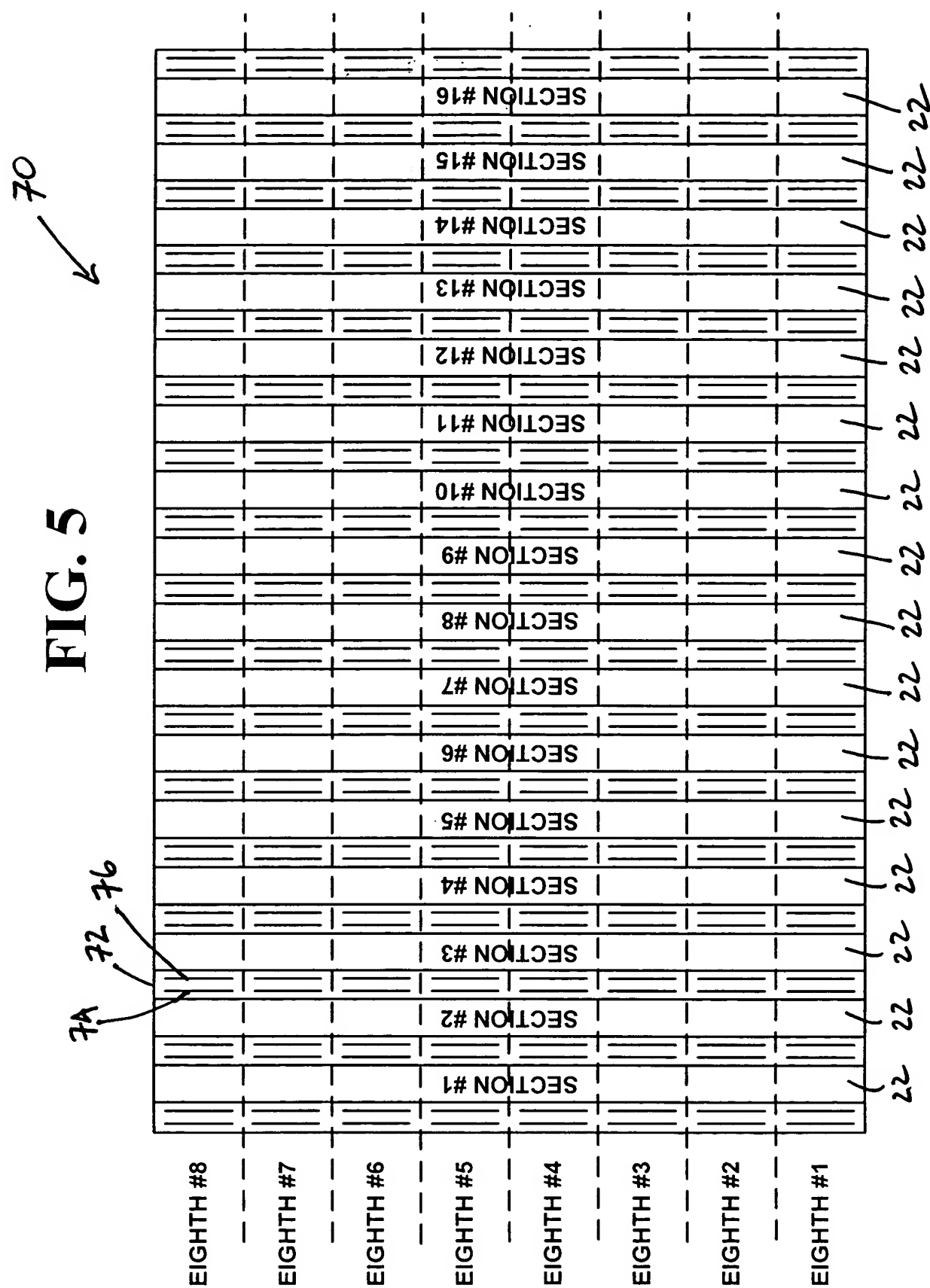
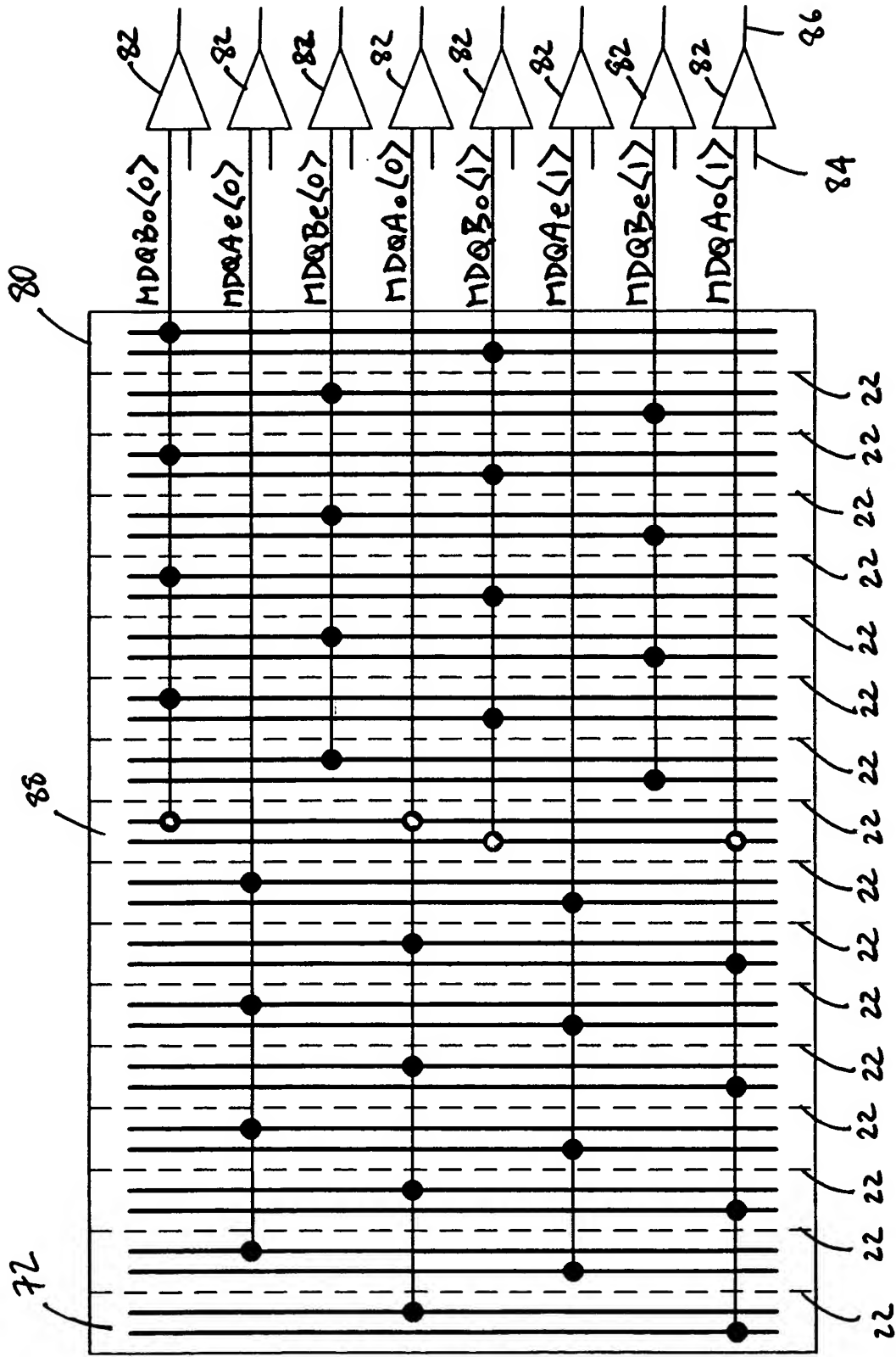


FIG. 4





The diagram illustrates a memory array with a grid of storage elements. Rows are connected to address lines 72, 80, and 86. Columns are connected to data lines 82 and 84. Specific column groups are labeled as MDQA0<0>, MDQAe<0>, MDQB0<0>, MDQBe<0>, MDQA0<1>, MDQAe<1>, MDQB0<1>, and MDQBe<1>. The array is divided into sections by dashed lines, suggesting a modular or hierarchical design.



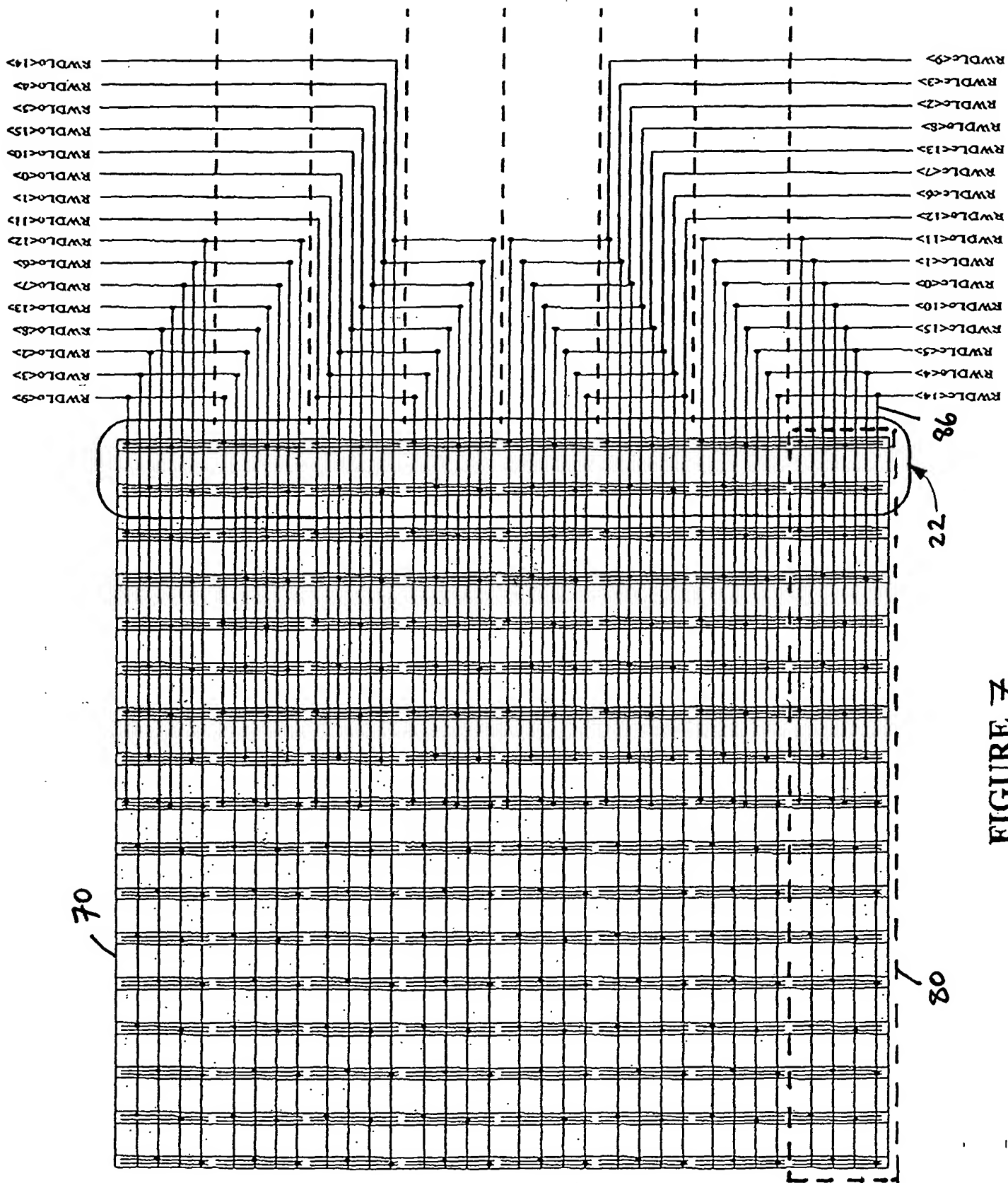


FIGURE 7

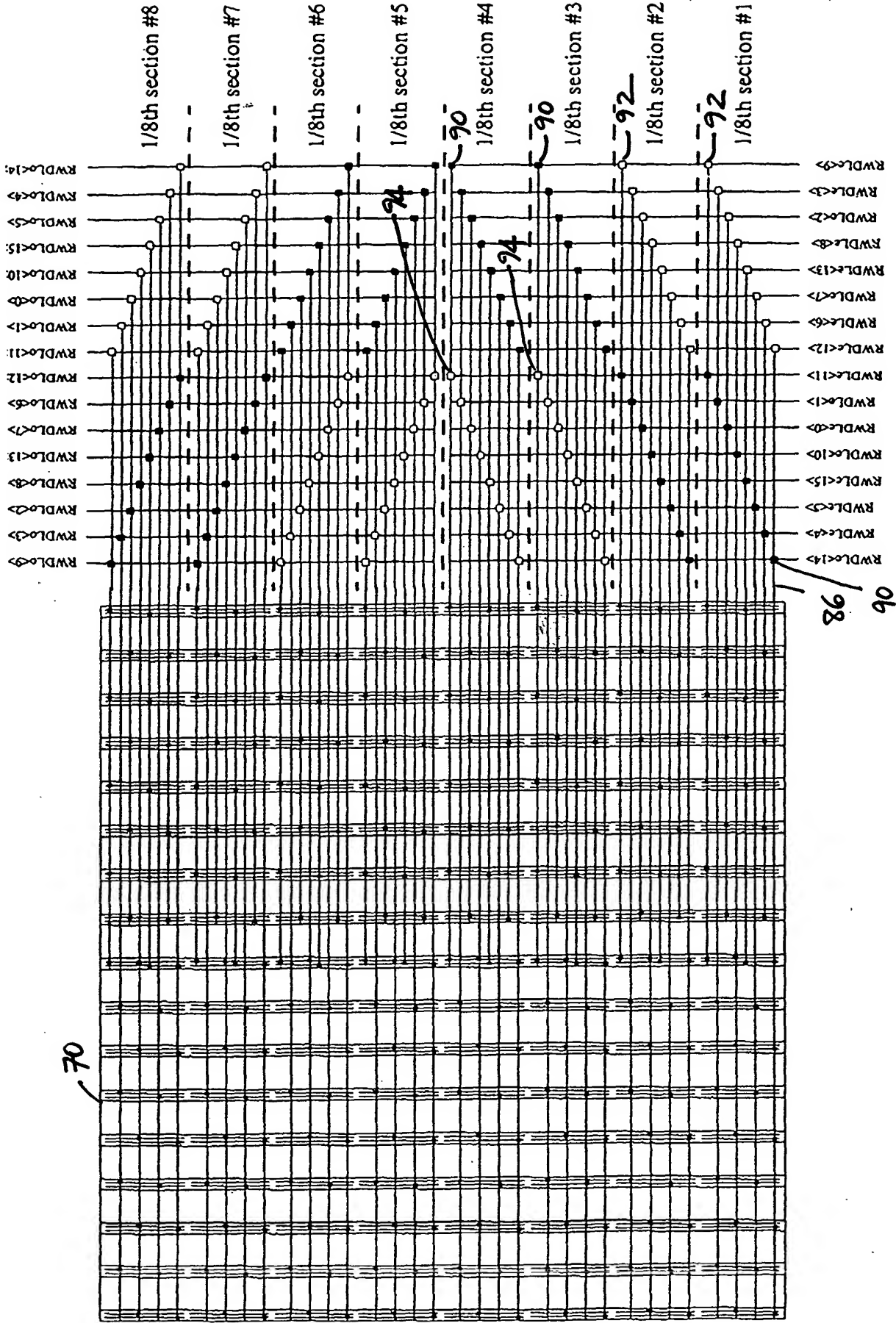


FIGURE 8



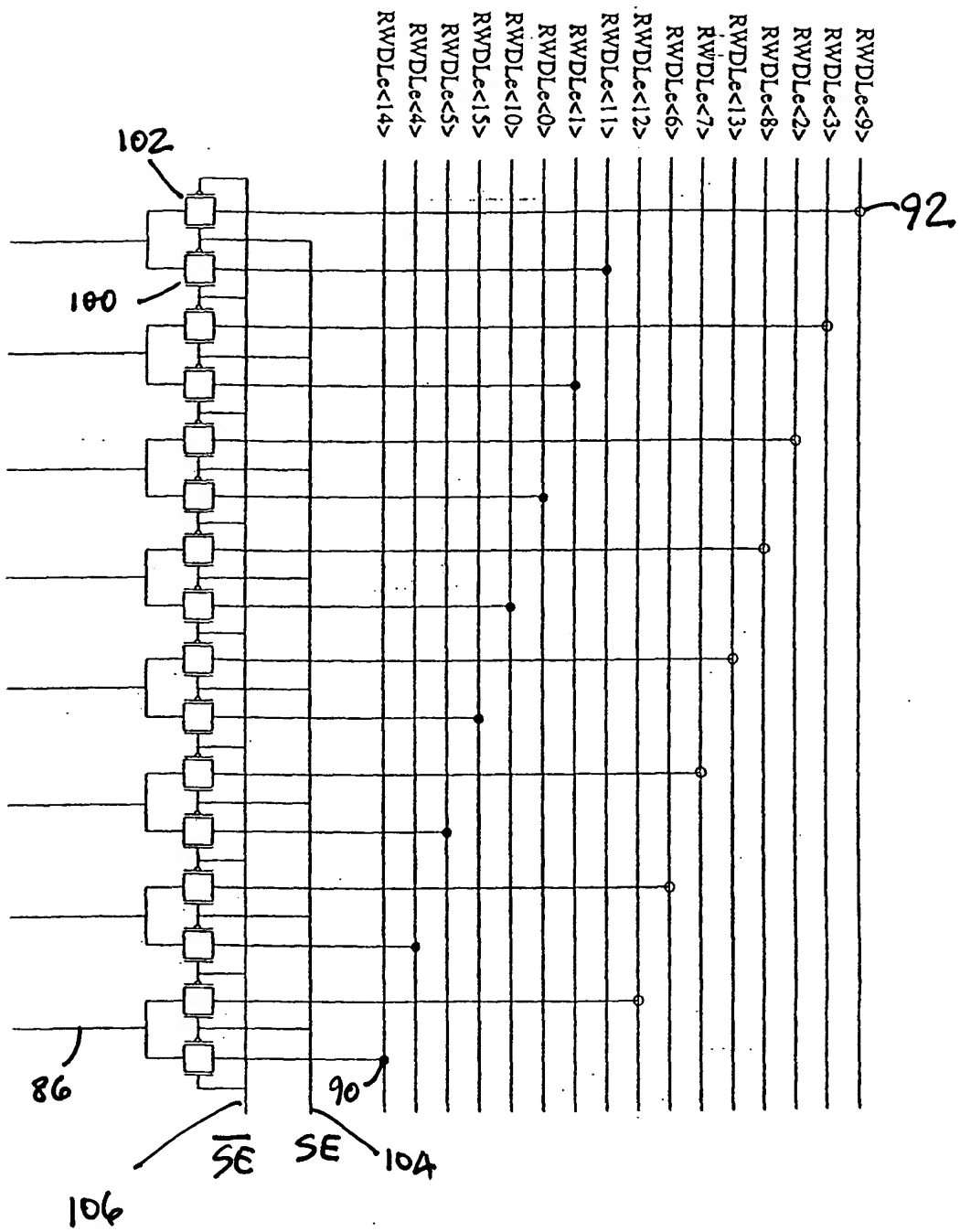


FIG. 9